







the valence band is designated by  $E_v$ . The separation between the energy of the lowest conduction band and that of the highest valence band is called the *bandgap energy*  $E_g$ , which is the most important parameter in semiconductors.

Electron energy is conventionally defined as positive when measured upward whereas the hole energy is positive when measured downward. A simplified band diagram is shown in Fig. 5-0-1.

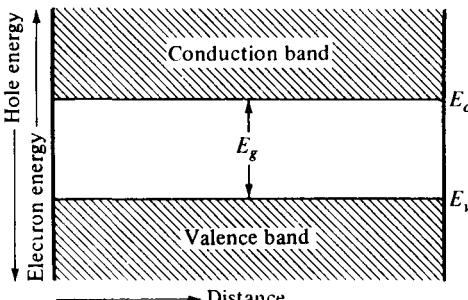


Figure 5-0-1 Energy-band diagram.

In the 1970s, it seemed that microwave transistors would be useful for generating power up to about 5 GHz. Since their inception, avalanche diodes have produced in excess of 4 W continuous wave (CW) at 5 GHz. Gunn diodes had been considered only for local oscillators or low-power transmitter applications, but recent results indicate that a single Gunn diode can generate an output power of 1 W at X band. At higher microwave frequencies, and even well into the millimeter range, limited space-charge-accumulation diodes (LSAS) can provide the highest peak power of any solid-state device, up to 250W in C band, 100 W in X band, and 50 W in Ku band. Since the pulsed Gunn and TRAPATT diodes are essentially transit-time devices, their operating frequency is approximately determined by the thickness of the active layer in the diode. An operating frequency of 10 GHz requires an active layer thickness on the order of 10  $\mu\text{m}$  (microns). Thus only a limited voltage can be applied to such a thin layer because of breakdown limitations. Consequently, the

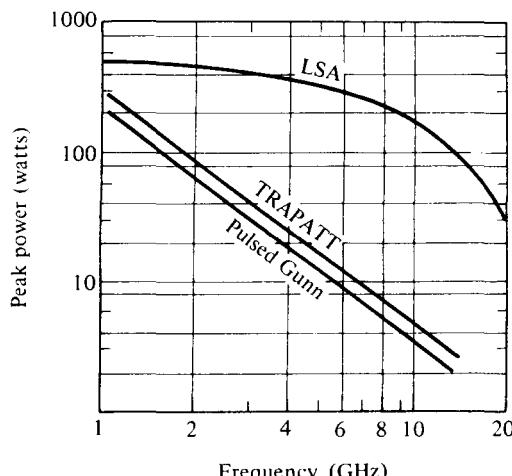


Figure 5-0-2 Peak-power levels achieved by microwave diode.

peak power capability of both the pulsed Gunn diodes and the TRAPATT diodes is greatly limited at higher frequencies. On the other hand, the peak power capability of an LSA diode is approximately proportional to the square of the thickness of the active layer because its operating frequency is independent of the thickness of the active layer. Thus the LSA diode is capable of producing higher peak power than either the pulsed Gunn diodes or the TRAPATT diodes. Figure 5-0-2 shows peak power versus frequency for these three devices.

Solid-state microwave power sources are widely used in radar, communications, navigational and industrial electronics, and medical and biological equipment. Representative applications for microwave solid-state devices are listed in Table 5-0-3.

**TABLE 5-0-3 APPLICATIONS OF MICROWAVE SOLID-STATE DEVICES**

Devices	Applications	Advantages
Transistor	L-band transmitters for telemetry systems and phased array radar systems	Low cost, low power supply, reliable, high CW power output, light weight
	L- and S-band transmitters for communications systems	
TED	C-, X-, and Ku-band ECM amplifiers for wideband systems	Low power supply (12 V), low cost, light weight, reliable, low noise, high gain
	X- and Ku-band transmitters for radar systems, such as traffic control	
IMPATT	Transmitters for millimeter-wave communications systems	Low power supply, low cost, reliable, high CW power output, light weight
TRAPATT	S-band pulsed transmitters for phased array radar systems	High peak and average power, reliable, low power supply, low cost
BARITT	Local oscillators in communications and radar receivers	Low cost, low power supply, reliable, low noise

## 5-1 MICROWAVE BIPOLAR TRANSISTORS

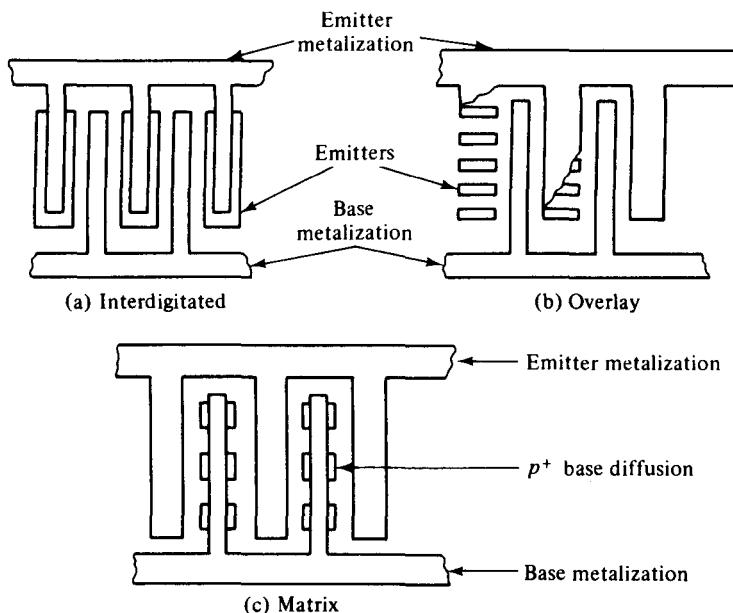
The invention of the transistor (contraction for transfer resistor) by William Shockley and his coworkers at Bell Laboratory in 1948 had a revolutionary impact on electronic technology in general and on solid-state devices in particular. Since then transistors and related semiconductor devices have replaced vacuum tubes for lower-power sources. Microwave power transistor technology has advanced significantly during the past three decades. The microwave transistor is a nonlinear device, and its principle of operation is similar to that of the low-frequency device, but requirements for dimensions, process control, heat sinking, and packaging are much more severe.

For microwave applications, the silicon (Si) bipolar transistors dominate for frequency range from UHF to about S band (about 3 GHz). As the technology improves, the upper frequency limit for these devices is continuously being extended, and at the present time the devices are capable of producing useful power up to 22 GHz. The majority of bipolar transistors of current interest are fabricated from silicon, although GaAs devices offer prospects for improvements in operating fre-

quency, in high temperatures, and in radiation hardness. The Si bipolar transistor is inexpensive, durable, integrative, and offers gain much higher than available with competing field-effect devices. It has moderate noise figure in RF amplifiers and 1/f noise characteristics that are about 10–20 dB superior to GaAs MESFETs. For these reasons, the Si bipolar transistors dominate in amplifier applications for the lower microwave frequencies and are often the devices of choice for local oscillators.

### 5-1-1 Physical Structures

All microwave transistors are now planar in form and almost all are of the silicon *n-p-n* type. The geometry can be characterized as follows: (a) interdigitated, (b) overlay, and (c) matrix (also called mesh or emitter grid) as shown in Fig. 5-1-1. The interdigitated type is for a small signal and power, but the overlay type and matrix type are for small power only. The figure of merit for the three surface geometries shown in Fig. 5-1-1 is listed in Table 5-1-1 [1].

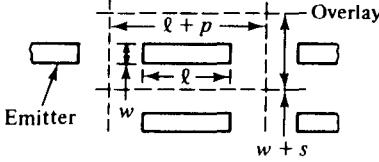
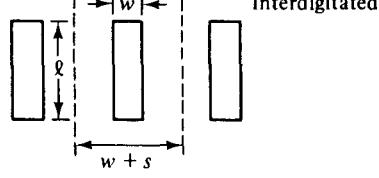
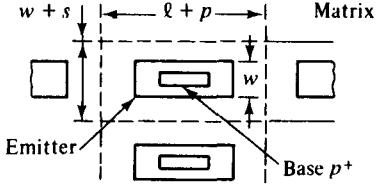


**Figure 5-1-1** Surface geometries of microwave power transistor. (From H. Sobol and F. Sterzer [1]; reprinted by permission of IEEE, Inc.)

For high-frequency applications, the *n-p-n* structure is preferred because the electron mobility ( $\mu_n = 1500 \text{ cm}^2/\text{V} \cdot \text{s}$ ) is much higher than the hole mobility ( $\mu_p = 450 \text{ cm}^2/\text{V} \cdot \text{s}$ ). Figure 5-1-2 shows an example of the densities for an *n-p-n* transistor. The density unit is in  $\text{cm}^2/\text{V} \cdot \text{s}$ .

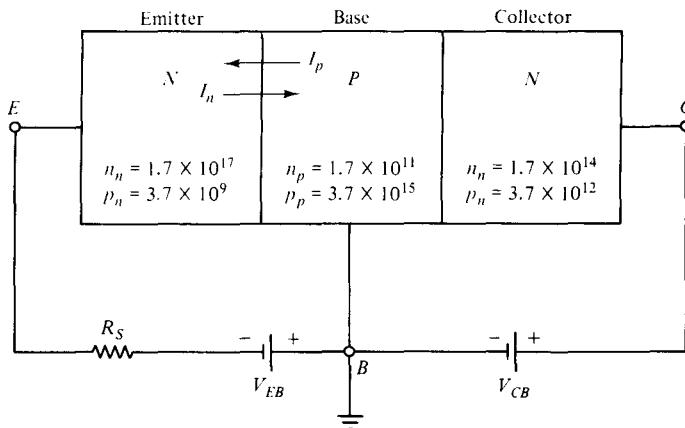
Although there are many ways of fabricating a transistor, diffusion and ion implantation are generally used. For example, the structure would typically start with a lightly doped *n*-type epitaxial layer as the collector. The base region would be formed by counter-doping the base region *p*-type by diffusion. The emitter would

**TABLE 5-1-1** FIGURE OF MERIT ( $M$ ) OF VARIOUS SURFACE GEOMETRIES

Surface geometry and unit cell	$M = \frac{EP}{BA}$
	$\frac{2(l+w)}{(w+s)(l+p)}$
	$\frac{2(l+w)}{l(w+s)}$
	$\frac{2(l+w)}{(w+s)(l+p)}$

Source: From H. Sobol and F. Sterzer [1]; reprinted by permission of IEEE, Inc.

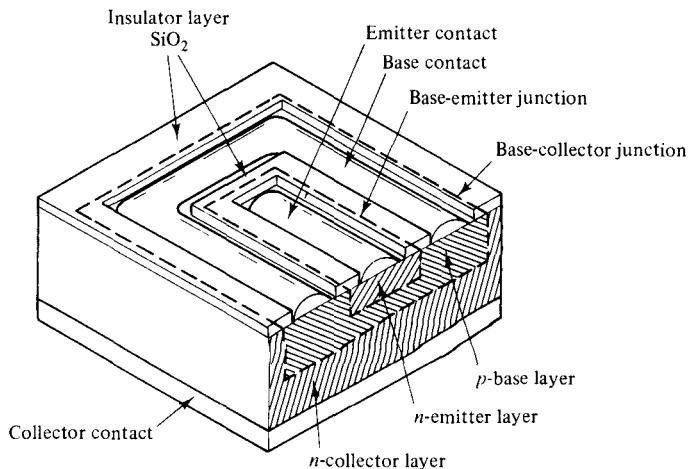
be formed by a shallow heavily doped  $n$ -type diffusion or by ion implantation. The emitter and base contacts are generally located on the semiconductor surface in an interdigital, planar arrangement. The interdigital geometry always provides for  $n + 1$  base fingers, where  $n$  is the number of emitter fingers. The number of fingers varies with the application, with more fingers required as the output power capabil-

**Figure 5-1-2** Carrier densities of an  $n-p-n$  transistor.

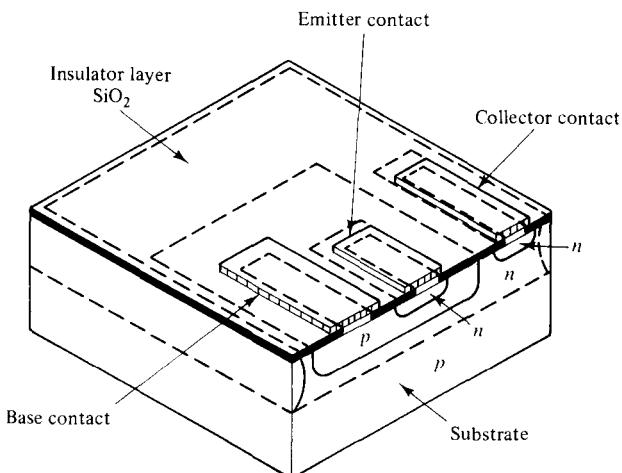
ity of the transistor increases. Additional fingers, however, increase the device parasitics and degrade the noise and upper frequency capability of the devices.

Figure 5-1-3 shows two schematic diagrams for a bipolar junction transistor (BJT): (a) the cross section of a discrete  $n-p-n$  planar BJT and (b) the cross section of a chip-type  $n-p-n$  integrated BJT.

The  $p$ - $n$ - $p$  bipolar junction transistor is a complementary structure of the  $n$ - $p$ - $n$  BJT by interchanging  $p$  for  $n$  and  $n$  for  $p$ . The  $p$ - $n$ - $p$  BJT is basically fabricated by first forming an  $n$ -type layer in the  $p$ -type substrate; then a  $p^+$ -type region is developed



(a) Discrete  $n-p-n$  planar BJT



**(b) Integrated chip-type  $n-p-n$  BJT**

**Figure 5-1-3** Schematic diagrams of bipolar junction transistors. (After D. Navon [2].)

oped in the *n* layer. Finally, metallic contacts are introduced to the *p*<sup>+</sup> region and *p* layer through the windows opened in the oxide layer and to the *p* region at the bottom.

### 5-1-2 Bipolar Transistor Configurations

In general, there are two types of bipolar transistors: *p-n-p* and *n-p-n*. In practical applications, a transistor can be connected as three different configurations: common base (CB), common emitter (CE), and common collector (CC), depending on the polarities of the bias voltages connected to its terminals.

**Common-base configuration.** The *common-base* (CB) configuration refers to the one where the emitter (input circuit) and collector (output circuit) terminals are common to the base as shown in Fig. 5-1-4.

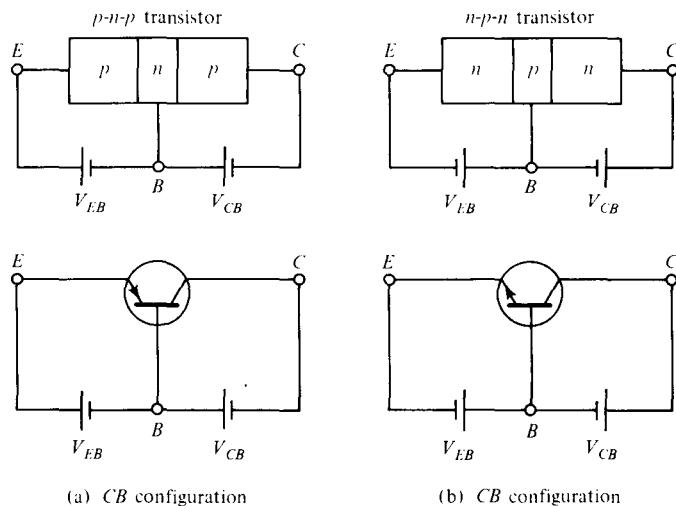


Figure 5-1-4 Common-base configurations for *p-n-p* and *n-p-n* transistors.

The CB configuration is also called the *grounded-base configuration*. For a *p-n-p* transistor, the largest current components are caused by holes. Holes flow from the emitter to the collector and down toward ground out of the base terminal. In an *n-p-n* transistor all current and voltage polarities are negative to those in a *p-n-p* transistor. The CB configuration of a transistor is usually used in amplifier applications. Its input voltage  $V_{EB}$  and output current  $I_C$  can be expressed in terms of the output voltage  $V_{CB}$  and input current  $I_E$  as

$$V_{EB} = \text{some function } (V_{CB}, I_E) \quad (5-1-1)$$

$$I_C = \text{some function } (V_{CB}, I_E) \quad (5-1-2)$$

**Common-emitter configuration.** Most transistors have their emitter, rather than their base, as the terminal to both input and output networks. Such a

configuration is known as *common-emitter* (CE) or *grounded-emitter configuration* as shown in Fig. 5-1-5.

In the CE configuration, the input current  $I_B$  and the output voltage  $V_{CE}$  are independent variables, whereas the input voltage  $V_{BE}$  and output current  $I_C$  can be written as

$$V_{BE} = \text{some function } (V_{CE}, I_B) \quad (5-1-3)$$

$$I_C = \text{some function } (V_{CE}, I_B) \quad (5-1-4)$$

The CE configuration is commonly used as a switch or pulse transistor amplifier. This is because the transistor is open at the cutoff mode and is closed at the saturation mode.

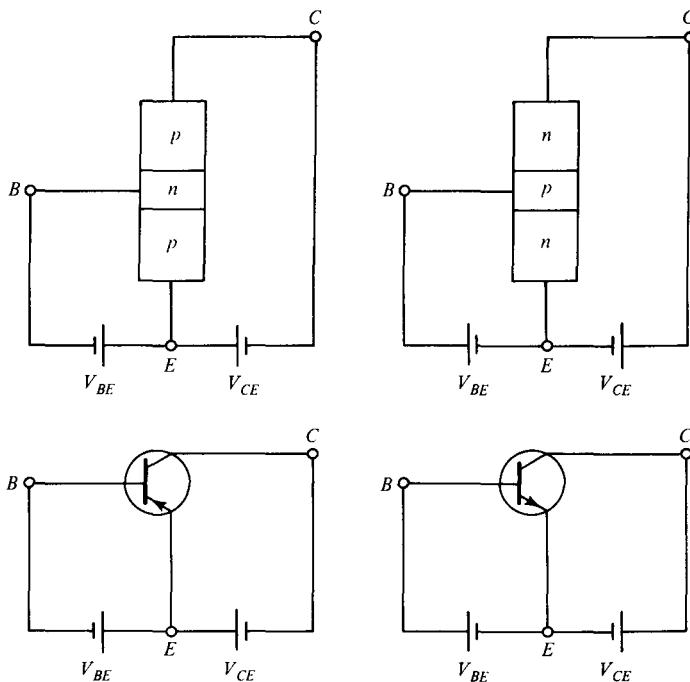


Figure 5-1-5 Common-emitter configurations for  $p-n-p$  and  $n-p-n$  transistors.

**Common-collector configuration.** Another transistor-circuit configuration is called the *common-collector* or *grounded-collector* configuration as shown in Fig. 5-1-6.

In a common-collector (CC) configuration, the output voltage of the load is taken from the emitter terminal instead of the collector as in the common-base and common-emitter configurations. When the transistor is cut off, no current will flow in the emitter terminal at the load. When the transistor is operating in a saturation mode, the load current reaches toward its maximum. Therefore the CC configuration transistor can also be used as a switch or pulse amplifier. The significant differ-

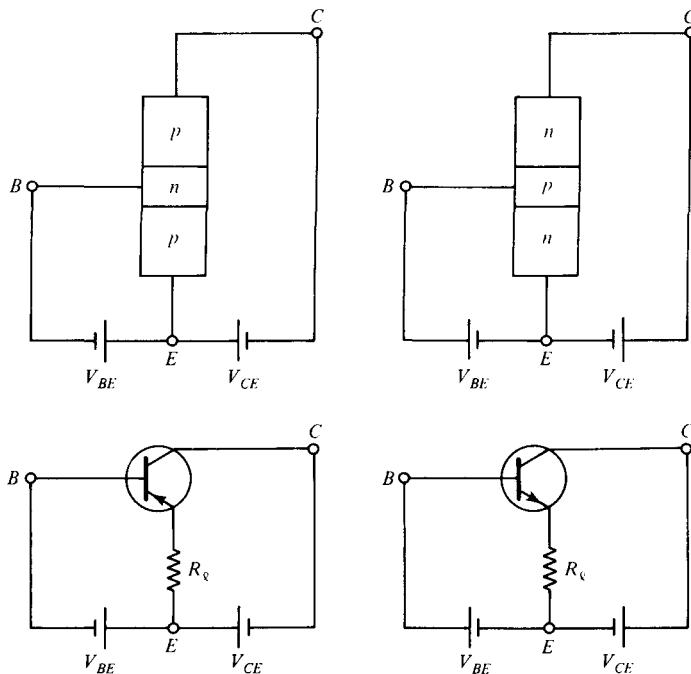


Figure 5-1-6 Common-collector configuration for  $p-n-p$  and  $n-p-n$  transistors.

ence, however, between common-emitter and common-collector configurations is that the common-collector amplifier has no voltage gain.

**Hybrid-pi equivalent model.** The *hybrid-pi equivalent model* is commonly used in the normal active mode of the common-emitter configuration for small-signal operation. Fig. 5-1-7 shows the hybrid-pi equivalent model of the common-emitter configuration.

For a small-signal operation, the nonlinear or ac parameters of a hybrid-pi equivalent model can be expressed as

$$v_{ce} = h_{ie} i_b + h_{re} v_{ce} \quad (5-1-5)$$

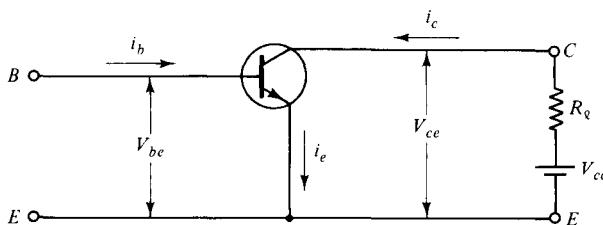
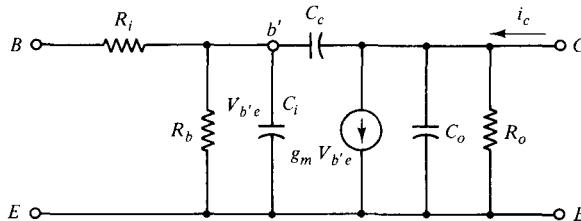
$$i_c = h_{fe} i_b + h_{oe} v_{ce} \quad (5-1-6)$$

$$\text{where } h_{ie} = \left. \frac{\partial v_{be}}{\partial i_b} \right|_{V_{ce}=\text{constant}} \quad (5-1-7)$$

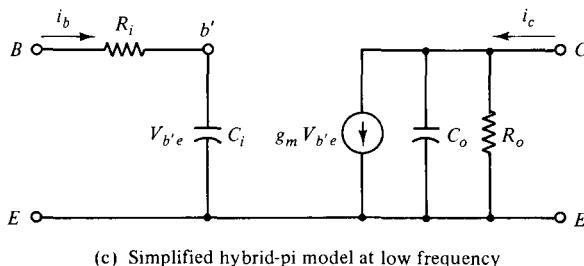
$$h_{re} = \left. \frac{\partial v_{be}}{\partial i_b} \right|_{i_b} \quad (5-1-8)$$

$$h_{fe} = \left. \frac{\partial i_c}{\partial i_b} \right|_{V_{ce}} \quad (5-1-9)$$

$$h_{oe} = \left. \frac{\partial i_c}{\partial v_{ce}} \right|_{i_b} \quad (5-1-10)$$

(a) Common-emitter *n*-*p*-*n* transistor

(b) Hybrid-pi model



(c) Simplified hybrid-pi model at low frequency

Figure 5-1-7 Hybrid-pi equivalent model.

When the dimensions of a bipolar junction transistor become very small, their  $Z$ ,  $Y$ , or  $H$  parameters cannot be measured because the input and output terminals cannot be openly and shortly realized. Therefore, the  $S$  parameters are commonly measured. In transistor design, it is necessary to convert the  $S$  parameters into  $Y$  parameters for the network component computations.

An incremental change of the emitter voltage  $\Delta V_{b'e}$  at the input terminal will induce an incremental change of the collector current  $\Delta i_c$  at the output terminal. Then the mutual conductance (or transconductance) of a small-signal transistor is defined by

$$g_m = \left. \frac{\partial i_c}{\partial V_{b'e}} \right|_{V_{ce}} \quad (5-1-11)$$

From the diode junction theory the thermal equilibrium density at the junction is equal to the minority density times the forward-bias voltage factor. That is,

$$n_p(0) = n_{po} e^{V_f/V_T} \quad (5-1-12)$$



Compute: (a) the mutual conductance  $g_m$ ; (b) the input conductance  $g_b$  and resistance  $R_i$ ; (c) the electron diffusion coefficient  $D_n$ ; and (d) the diffusion capacitance  $C'_{be}$ .

### Solution

a. The mutual conductance is

$$g_m = \frac{I_c}{V_T} = \frac{6 \times 10^{-3}}{26 \times 10^{-3}} = 0.23 \quad \text{mho}$$

b. The input conductance and resistance are

$$g_b = \frac{g_m}{h_{FE}} = \frac{0.23}{120} = 1.92 \times 10^{-3} \quad \text{mho}$$

$$R_i = 521 \quad \text{ohms}$$

c. The electron diffusion coefficient is

$$D_n = \mu_n \frac{KT}{q} = \mu_n V_T = 1600 \times 26 \times 10^{-3} = 41.6 \text{ cm}^2/\text{s}$$

d. The diffusion capacitance is

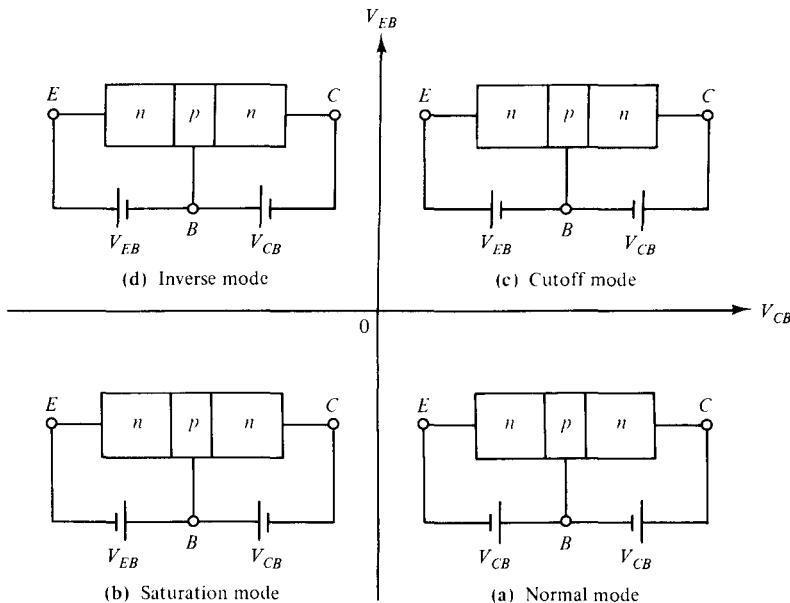
$$C'_{be} = g_m \frac{W_b^2}{2D_n} = 0.23 \times \frac{10^{-8}}{2 \times 41.6} = 2.76 \text{ pF}$$

### 5-1-3 Principles of Operation

The bipolar junction transistor (BJT) is an active three-terminal device which is commonly used as an amplifier or switch. Its principles of operation are discussed in this section.

**Modes of operation.** A bipolar transistor can operate in four different modes depending on the voltage polarities across the two junctions: normal (active) mode, saturation mode, cutoff mode, and inverse (or inverted) mode as shown in Fig. 5-1-8.

- Normal Mode.** If the emitter junction of an  $n-p-n$  transistor is forward-biased and the collector is reverse-biased, the transistor is operated in the normal mode as shown in Fig. 5-1-8(a). The term *forward bias* means that the positive polarity of the bias voltage is connected to the  $p$  side and the negative polarity to the  $n$  side for a  $p-n$  junction; the opposite obtains for reverse bias. Most transistor amplifiers are operated in normal mode, and its common-base current gain *alpha* is known as the *normal alpha*  $\alpha_N$ .
- Saturation Mode.** When both transistor junctions are forward-biased, the transistor is in its saturation mode with very low resistance, and acts like a short circuit, as shown in Fig. 5-1-8(b).
- Cutoff Mode.** If both transistor junctions are reverse-biased the transistor is operated in its cutoff mode. As the current is cut off, the transistor acts like an

Figure 5-1-8 Operational modes of an  $n-p-n$  transistor.

open circuit. Both the cutoff and saturation modes of a transistor are used as switching devices for the OFF and ON states. Fig. 5-1-8(c) shows the cutoff-mode bias-voltage connection.

4. **Inverse Mode.** When the emitter is reverse-biased and the collector is forward-biased, the transistor is operated in the inverse (or inverted) mode, and its current gain is designated as the *inverse alpha*  $\alpha_I$ . If the transistor is symmetric, the *normal alpha*  $\alpha_N$  is nearly equal to the inverse alpha  $\alpha_I$ . The two current gains, however, are not actually equal because of their unequal dopings. The inverse mode is shown in Fig. 5-1-8(d). In practice, the inverse mode is not commonly used except as a multiemitter transistor in TTL (transistor-transistor logic) logic gate.

**Current flow in normal mode.** When a transistor is properly biased, the holes and electrons in the transistor will follow the field direction in motion. Figure 5-1-9 shows the current flow of an  $n-p-n$  transistor.

The current flow in an ideal  $n-p-n$  bipolar junction transistor is analyzed under the following assumptions:

1. The resistivities of the semiconductor regions are low
2. The injected current densities are low
3. The space-charge layer widening effects can be ignored
4. The current and voltage of  $n-p$  junction diodes follow the basic equation of

$$I = I_o(e^{V/V_T} - 1) \quad (5-1-20)$$

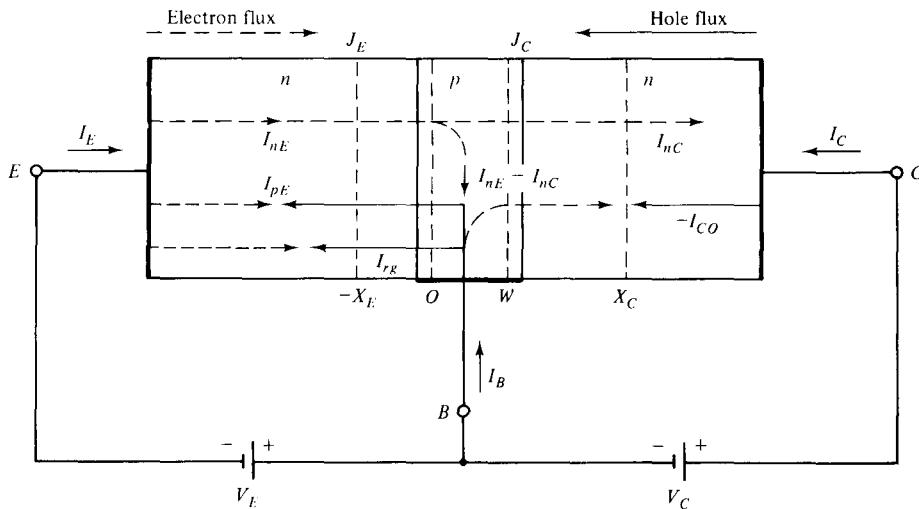


Figure 5-1-9 Current flow in an *n-p-n* transistor.

For a common-base *n-p-n* transistor, the emitter junction is forward-biased and the collector junction is reverse-biased as shown in Fig. 5-1-9. Consequently, the emitter current  $I_E$  consists of electron current  $I_{nE}$  crossing from the emitter into the base and the hole current  $I_{pE}$  crossing from the base into the emitter. Since the doping of the emitter is much larger than the doping of the base, the hole current is negligible. However, not all the electrons crossing the emitter junction  $J_E$  reach the collector junction  $J_C$  because some of them combine with the holes in the *p*-type base. If  $I_{nE}$  is the electron current at the collector junction  $J_C$ , there must be a recombination current  $I_{nE} - I_{nC}$  leaving the base. When the emitter is open-circuited, then  $I_E = 0$  and  $I_{nC} = 0$ . As a result, the collector current  $I_C$  is equal to the reverse saturation current  $I_{CO}$  because the junction between base and collector is reverse-biased. From Fig. 5-1-9, we have

$$I_B = I_{pE} - (I_{nE} - I_{nC}) - I_{CO} + I_{rg} \quad (5-1-21)$$

$$I_E = -I_{pE} + I_{nE} - I_{rg} \quad (5-1-22)$$

and

$$I_C = -I_{CO} - I_{nC} \quad (5-1-23)$$

For an *n-p-n* transistor,  $I_{CO}$  consists of holes moving across the collector junction  $J_C$  from right to left (collector to base) and electrons crossing  $J_C$  in the opposite direction. Since the reference direction for  $I_{CO}$  in Fig. 5-1-9 is assumed from left to right, then, for an *n-p-n* transistor,  $I_{CO}$  is positive for forward-biased  $J_C$  junction and  $I_{CO}$  is negative for reverse-biased  $J_C$  junction. The saturation current  $I_{CO}$  at the  $J_C$  junction of an *n-p-n* transistor is given by

$$I_{CO} = \frac{AqDn_{po}}{W} + \frac{AqD_p p_{no}}{L_E} = Aqn_i^2 \left( \frac{D_n}{WN_a} + \frac{D_p}{L_E N_d} \right) \quad (5-1-24)$$

Also from Fig. 5-1-9, the sum of the three terminal currents should be zero and it is

$$I_E + I_C + I_B = 0 \quad (5-1-25)$$

Equation (5-1-25) can be verified by adding together Eqs. (5-1-21) through (5-1-23).

**Current flow in common-base *n-p-n* transistor.** In a common-base configuration of an *n-p-n* transistor as shown in Fig. 5-1-9, the emitter *n-p* junction is forward-biased and the collector *p-n* junction is reverse biased. Their total current flow can be found from the basic diffusion equation. The steady-state diffusion equation for an *n-p-n* transistor at low-level injection is given by

$$I_n = AqD_n \frac{dn_p}{dx} \quad (5-1-25a)$$

and

$$D_n = \frac{d^2 n_p}{dx^2} - \frac{n_p - n_{po}}{\tau_n} = 0 \quad (5-1-26)$$

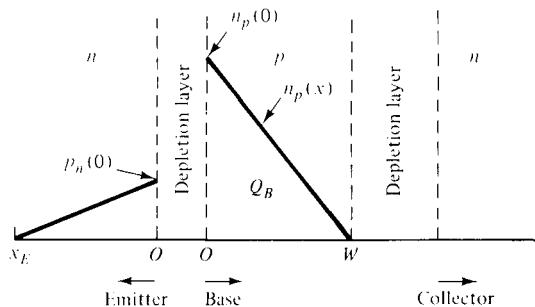
where  $D_n$  = electron diffusion constant

$n_p$  = minority electron carrier density in the *p*-type base layer

$n_{po}$  = equilibrium minority electron carrier density in the *p*-type base layer

$x$  = distance measured from the base region as shown in Fig. 5-1-10

$\tau_n$  = electron lifetime



**Figure 5-1-10** Minority-carrier densities under normal active bias with negligible recombination.

The general solution of Eq. (5-1-26) can be written as

$$n_p - n_{po} = C_1 e^{-x/L_n} + C_2 e^{x/L_n} \quad (5-1-27)$$

where  $C_1$  and  $C_2$  are constants to be determined by the boundary conditions

$L_n = \sqrt{\tau_n D_n}$  is the electron diffusion length

$n_{po} = n_i^2/N_a$  is the mass-action law

The boundary conditions at the edge of the emitter depletion layer in the base side with a forward-biased emitter junction is

$$n_p(0) = n_{po} e^{V_E/V_T} \quad (5-1-28)$$

where  $V_E$  = forward-biased voltage across the emitter junction

$V_T = 26 \times 10^{-3}$  V at  $300^\circ$  K is the voltage equivalent of temperature

The boundary condition at the depletion-layer edge of the reverse-biased collector junction is usually assumed to be

$$n_p(W) = 0 \quad (5-1-29)$$

The two boundary conditions are shown in Fig. 5-1-10.

The general solution of Eq. (5-1-26) can be written as

$$n_p(x) = n_{po} \left( e^{V_E/V_T} - 1 \right) \left[ \frac{\sinh [(W-x)/L_n]}{\sinh (W/L_n)} + n_{po} \left( 1 - \frac{\sinh (x/L_n)}{\sinh (W/L_n)} \right) \right] \quad (5-1-30)$$

In almost all transistors, the base width is made very narrow ( $W \ll L_n$ ) so that the minority-carrier recombination in the base is negligible. As a result, the boundary conditions specify the two end points of the base carrier concentration with a straight line as shown in Fig. 5-1-11. (Note:  $\sinh y \doteq y$ ,  $\cosh y \doteq 1$ ,  $\coth y \doteq 1/y$ , and  $\operatorname{sech} y \doteq 1 - y^2/2$  for  $y \ll 1$ .)

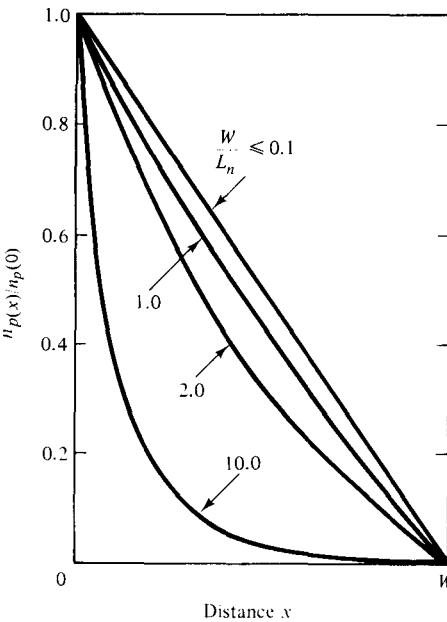


Figure 5-1-11 Minority carrier distributions in base region as a function of  $W/L_n$ . (After S. Sze [3].)

For  $W \ll L_n$ , the minority carrier distribution of Eq. (5-1-30) can be simplified to

$$n_p(x) = n_p(0) \left( 1 - \frac{x}{W} \right) = n_{po} e^{V_E/V_T} \left( 1 - \frac{x}{W} \right) \quad (5-1-31)$$

Then the boundary conditions for holes in the emitter and collector depletion regions can be expressed, respectively, as

$$p_E = p_{EO} e^{V_E/V_T} \quad \text{at } x = -x_E \quad (5-1-32)$$

and

$$p_C = p_{CO} e^{-V_C/V_T} \quad \text{at } x = x_C \quad (5-1-33)$$

where  $p_{EO}$  = equilibrium minority hole density in the emitter region

$p_{CO}$  = equilibrium minority hole density in the collector region

Substituting Eqs. (5-1-32) and (5-1-33) into Eq. (5-1-27) yields the minority distributions in the emitter and collector regions as

$$p_E(x) = p_{EO} + p_{EO}(e^{V_E/V_T} - 1) \exp [(x + x_E)/L_n] \quad \text{for } x \leq -x_E \quad (5-1-34)$$

and

$$p_C(x) = p_{CO} + p_{CO} \exp [-(x - x_C)/L_n] \quad \text{for } x \geq x_C \quad (5-1-35)$$

The total excess minority-carrier charge in the base region is given by

$$Q_B = Aq \int_0^W [n_p(x) - n_{po}(x)] dx \simeq \frac{AqWn_p(0)}{2} \quad (5-1-36)$$

where  $A$  = cross section

The base recombination current for a carrier lifetime  $\tau_n$  is

$$I_{nB} = \frac{AQ_B}{\tau_n} = \frac{AqWn_{po}}{2\tau_n} e^{V_E/V_T} \quad (5-1-37)$$

According to the carrier injection processes, the minority electron density at the reverse-biased collector junction  $J_C$  is usually assumed to be zero. That is,

$$n_{pC} = 0 \quad \text{at } J_C \text{ for } x = W \quad (5-1-38)$$

This assumption is reasonable because the electric field of the collector junction sweeps carriers into the collector so that the collector is almost a perfect sink.

The electron current  $I_{nE}$  which is injected from the emitter into the base at  $x = 0$  for  $L_n \gg W$  is proportional to the gradient of the minority carrier density and is expressed as

$$\begin{aligned} I_{nE} &= AqD_n \frac{dn_p}{dx} \Big|_{x=0} = \frac{-AqD_n n_{po}}{L_n} \coth (W/L_n) \left[ (e^{V_E/V_T} - 1) + \frac{1}{\cosh (W/L_n)} \right] \\ &= \frac{-AqD_n n_i^2}{N_a W} (e^{V_E/V_T} - 1) - \frac{AqD_n n_i^2}{N_a W} \doteq -\frac{AqD_n n_i^2}{N_a W} e^{V_E/V_T} \end{aligned} \quad (5-1-39)$$

The electron current which reaches the collector at  $x = W$  is

$$\begin{aligned} I_{nC} &= Aq \frac{dn_p}{dx} \Big|_{x=W} = \frac{-AqD_n n_{po}}{L_n} \frac{1}{\sinh (W/L_n)} \left[ (e^{V_E/V_T} - 1) + \cosh (W/L_n) \right] \\ &= \frac{-AqD_n n_i^2}{N_a W} (e^{V_E/V_T} - 1) - \frac{AqD_n n_i^2}{N_a W} = -\frac{AqD_n n_i^2}{N_a W} e^{V_E/V_T} \end{aligned} \quad (5-1-40)$$

The collector current  $I_{nC}$  can also be expressed as

$$\begin{aligned}
 I_{nC} &= I_{nE} - I_{nB} = I_{nE} \left( 1 - \frac{I_{nB}}{I_{nE}} \right) \\
 &= I_{nE} \left( 1 - \frac{W^2}{2\tau_n D_n} \right) = I_n^E \left( 1 - \frac{W^2}{2L_E^2} \right)
 \end{aligned} \tag{5-1-41}$$

where  $L_E$  = diffusion length of the emitter and  $\exp(V_E/V_T) \gg 1$  is assumed

Similarly, the hole currents are

$$I_{pE} = \frac{AqD_E p_{EO}}{L_E} (e^{V_E/V_T} - 1) \quad \text{for } x = -x_E \tag{5-1-42}$$

and

$$I_{pC} = \frac{AqD_C p_{CO}}{L_C} \quad \text{for } x = x_C \tag{5-1-43}$$

where  $D_E$  and  $D_C$  are the hole diffusion constants in the emitter and collector, respectively

$L_C$  = diffusion length of the collector

The current flow in an  $n-p-n$  transistor as described so far is an ideal model, and its recombination-generation current is not counted. If the recombination current is considered, the current flow is the sum of the drift, the diffusion, and the recombination-generation currents. That is,

$$I = I_{dr} \text{ (drift)} + I_{df} \text{ (diffusion)} + I_{rg} \text{ (recombination-generation)} \tag{5-1-44}$$

The recombination-generation current can be computed from the following equation

$$I_{rg} = \frac{Aq n_i x_d}{\tau_o} e^{V_E/(2V_T)} \tag{5-1-45}$$

where  $x_d$  = depletion-layer width

$\tau_o$  = effective minority-carrier lifetime in the depletion layer

Figure 5-1-12 shows current-voltage (I-V) characteristics of an ideal  $n-p-n$  bipolar transistor for a common-base configuration.

There are three regions for the I-V characteristics of an  $n-p-n$  bipolar transistor:

- Active Region:** In this region the emitter junction is forward-biased and the collector junction is reverse-biased. The collector current  $I_C$  is essentially independent of collector voltage and depends only on the emitter current  $I_E$ . When the emitter current is zero, the collector current is equal to the reverse saturation current  $I_{Co}$ .
- Saturation Region:** In this region, as shown on the left side of Fig. 5-1-12, both emitter and collector junctions are forward-biased. The electron current flows from the  $n$  side across the collector junction to the  $p$ -type base. As a result, the collector current increases sharply.

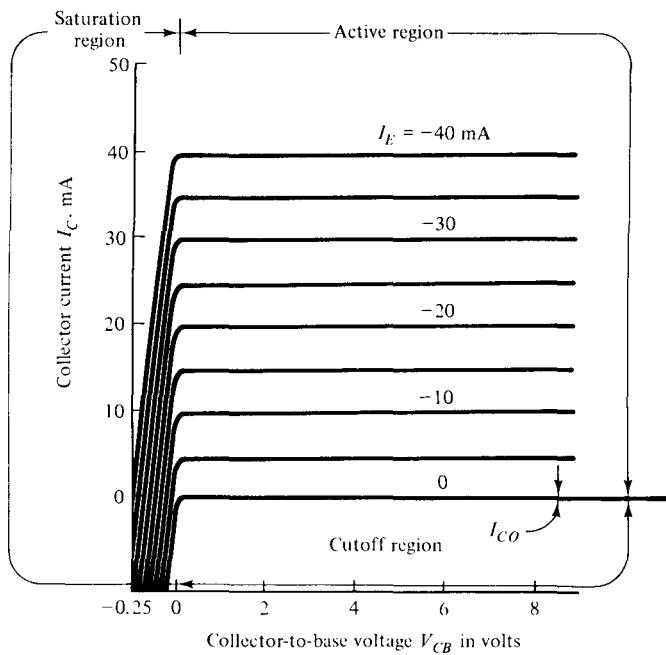


Figure 5-1-12 Current-Voltage (I-V) characteristics of an *n-p-n* transistor.

**3. Cutoff Region:** In this region the emitter and collector junctions are both reverse-biased. Consequently, the emitter current is cut off to zero, as shown in the lower right side of Fig. 5-1-12.

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**Example 5-1-2: I-V Characteristics of an *n-p-n* Transistor**

A silicon *n-p-n* transistor at 300° K has the following parameters:

Base width:	$w = 10^{-5}$ cm
Diffusion length in emitter:	$L_E = 10^{-4}$ cm
Diffusion length in collector:	$L_C = 5 \times 10^{-4}$ cm
Base resistivity:	$\rho_B = 0.15 \Omega\text{-cm}$
Emitter resistivity:	$\rho_E = 0.006 \Omega\text{-cm}$
Collector resistivity:	$\rho_C = 16 \Omega\text{-cm}$
Emitter junction voltage:	$V_E = 0.5$ V
Collector junction voltage:	$V_C = 0.6$ V
Cross-section area:	$A = 2 \times 10^{-2}$ cm <sup>2</sup>

Find:

- The impurity densities in the emitter, base, and collector regions
- The mobilities in the emitter, base, and collector regions
- The diffusion lengths in the emitter, base, and collector regions

d. The equilibrium densities in the emitter, base, and collector regions  
 e. The terminal currents

**Solution**

a. The impurity densities are read from Fig. A-1 in Appendix A as

$$N_{dE} = 1 \times 10^{19} \text{ cm}^{-3} \quad \text{in the } n\text{-type emitter region}$$

$$N_{aB} = 1.5 \times 10^{17} \text{ cm}^{-3} \quad \text{in the } p\text{-type base region}$$

$$N_{dC} = 3 \times 10^{14} \text{ cm}^{-3} \quad \text{in the } n\text{-type collector region}$$

b. The mobilities are read from Fig. A-2 in Appendix A as

$$\mu_{pE} = 80 \text{ cm}^2/\text{V}\cdot\text{s} \quad \text{in the emitter}$$

$$\mu_{nE} = 105 \text{ cm}^2/\text{V}\cdot\text{s} \quad \text{in the emitter}$$

$$\mu_{pB} = 400 \text{ cm}^2/\text{V}\cdot\text{s} \quad \text{in the base}$$

$$\mu_{nC} = 1600 \text{ cm}^2/\text{V}\cdot\text{s} \quad \text{in the collector}$$

c. The diffusion constants are computed to be

$$D_{pE} = \mu_{pE}V_T = 80 \times 26 \times 10^{-3} = 2.08 \text{ cm}^2/\text{s}$$

$$D_{nE} = \mu_{nE}V_T = 105 \times 26 \times 10^{-3} = 2.73 \text{ cm}^2/\text{s}$$

$$D_{pB} = \mu_{pB}V_T = 400 \times 26 \times 10^{-3} = 10.4 \text{ cm}^2/\text{s}$$

$$D_{nC} = \mu_{nC}V_T = 1600 \times 26 \times 10^{-3} = 41.6 \text{ cm}^2/\text{s}$$

d. The equilibrium densities are

$$n_{PB} = n_i^2/N_{aB} = (1.5 \times 10^{10})^2/(1.5 \times 10^{17}) = 1.5 \times 10^3 \text{ cm}^{-3}$$

$$p_{EO} = n_i^2/N_{dE} = (1.5 \times 10^{10})^2/(1 \times 10^{19}) = 2.5 \times 10^4 \text{ cm}^{-3}$$

$$p_{CO} = n_i^2/N_{dC} = (1.5 \times 10^{10})^2/(3 \times 10^{14}) = 7.5 \times 10^5 \text{ cm}^{-3}$$

e. The terminal currents are computed as follows:

From Eq. (5-1-39), the electron current in the emitter is

$$\begin{aligned} I_{nE} &= -\frac{AqD_n n_i^2}{N_a W} e^{V_E/V_T} = \frac{A_q D_p n_i^2}{L_E N_d} (e^{V_E/V_T} - 1) \\ &= -\frac{2 \times 10^{-2} \times 1.6 \times 10^{-19} \times 2.73 \times (1.5 \times 10^{10})^2}{1.5 \times 10^{17} \times 10^{-5}} \\ &\quad \times \exp[0.5/(26 \times 10^{-3})] \\ &= -13.104 \times 10^{-13} \times 2.248 \times 10^8 \\ &= -0.2946 \text{ mA} \end{aligned}$$

From Eq. (5-1-42), the hole current in the emitter is

$$\begin{aligned} I_{pE} &= \frac{AqD_E p_{EO}}{L_E} (e^{V_E/V_T} - 1) = \frac{AqD_p n_i^2}{L_E N_d} (e^{V_E/V_T} - 1) \\ &= \frac{2 \times 10^{-2} \times 1.6 \times 10^{-19} \times 2.08 \times (1.5 \times 10^{10})^2}{10^{-4} \times 1 \times 10^{19}} \times (2.248 \times 10^8 - 1) \\ &= 14.976 \times 10^{-16} \times 2.248 \times 10^8 \\ &= 0.337 \mu\text{A} \end{aligned}$$

From Eq. (5-1-24), the reverse saturation current in the collector is

$$\begin{aligned}
 I_{CO} &= \frac{-AqD_n n_i^2}{N_a W} - \frac{AqD_p p_{no}}{L_E} \\
 &= -13.104 \times 10^{-13} - 14.976 \times 10^{-16} \\
 &= -1.312 \text{ pA}
 \end{aligned}$$

From Eq. (5-1-40), the electron current which reaches the collector is

$$\begin{aligned}
 I_{nC} &= -\frac{AqD_n n_i^2}{N_a W} e^{V_E/V_T} = -13.104 \times 10^{-13} \times 2.248 \times 10^8 \\
 &= -0.2946 \text{ mA}
 \end{aligned}$$

The emitter current is

$$\begin{aligned}
 I_E &= -I_{pE} + I_{nE} = -33.67 \times 10^{-8} - 0.295 \times 10^{-3} \\
 &= -0.295 \text{ mA}
 \end{aligned}$$

The collector current is

$$\begin{aligned}
 I_C &= -I_{CO} - I_{nC} = 1.312 \times 10^{-12} - (-0.295 \times 10^{-3}) \\
 &= 0.295 \text{ mA}
 \end{aligned}$$

The current in the base terminal is

$$\begin{aligned}
 I_B &= I_{pE} - (I_{nE} - I_{nC}) + I_{CO} \\
 &= 33.67 \times 10^{-8} - (-29.46 \times 10^{-5} + 29.46 \times 10^{-5}) + 1.312 \times 10^{-12} \\
 &= 0.337 \mu\text{A}
 \end{aligned}$$

Note: The recombination-generation currents in the space-charge regions are not counted.

#### 5-1-4 Amplification Phenomena

Bipolar transistors are usually used for signal amplification. The amplification phenomena can be described from the common-base and common-emitter transistors.

**Common-base *n-p-n* transistor.** The ratio of the output current to the input current for a small signal in a bipolar junction transistor is known as the *current gain alpha*  $\alpha$ , or  $h_{fb}$ . The current gain of a common-base *p-n-p* transistor is defined by the current components crossing the emitter and collector junctions as

$$\alpha = -\frac{I_C + I_{CO}}{I_E} = h_{fb} \quad (5-1-46)$$

where  $I_{CO}$  = collector-junction reverse saturation current with zero emitter current

Since  $I_C$  and  $I_E$  have opposite signs, the alpha  $\alpha$ , as defined, is always positive. Typical numerical values of  $\alpha$  are between 0.9 and 0.995.

The emitter efficiency (or injection efficiency) is defined as

$$\begin{aligned}\gamma &= \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}} \\ &= \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{1}{1 + I_{pE}/I_{nE}} = \left(1 + \frac{D_p N_a W}{D_n N_d L_E}\right)^{-1}\end{aligned}\quad (5-1-47)$$

where  $I_{nE}$  = injected electron diffusion current at emitter junction  $J_E$   
 $I_{pE}$  = injected hole diffusion current at emitter junction  $J_E$

The transport factor  $\beta^*$  is defined as

$$\begin{aligned}\beta^* &= \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current at } J_E} \\ &= \frac{I_{nC}}{I_{nE}} = 1 - \frac{W^2}{2\tau_n D_n} = 1 - \frac{W^2}{2L_n^2}\end{aligned}\quad (5-1-48)$$

where  $I_{nC}$  = injected electron diffusion current at  $J_C$

$I_{nE}$  = injected electron diffusion current at  $J_E$

$L_n = \sqrt{\tau_n D_n}$  is the electron diffusion length

At the collector we have

$$I_C = -I_{CO} - I_{nC} \quad (5-1-49)$$

Then the current gain can be expressed as

$$\alpha = \frac{I_{nC}}{I_E} = \beta^* \gamma \quad (5-1-50)$$

In the normal active mode, the collector current is given by

$$I_C = -\alpha I_E - I_{CO} \quad (5-1-51)$$

The current  $I_{CO}$  is the current crossing the  $p-n$  junction, and it is expressed in Eq. (5-1-24). Then the complete expression of  $I_C$  for any  $V_C$  and  $I_E$  is

$$I_C = -\alpha I_E + I_{CO}(1 - e^{V_C/V_T}) \quad (5-1-52)$$

where  $I_O = -I_{CO}$  is replaced.

### Example 5-1-3: Silicon Bipolar Transistor

A silicon  $n-p-n$  bipolar transistor operates in common-base mode at  $300^\circ \text{ K}$  and has the following parameters:

Silicon intrinsic density:	$n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$
Acceptor density in base region:	$N_a = 5 \times 10^{16} \text{ cm}^{-3}$
Donor density in emitter region:	$N_d = 5 \times 10^{18} \text{ cm}^{-3}$
Hole lifetime:	$\tau_p = 1 \mu\text{s}$

Electron lifetime:	$\tau_n = 1$	$\mu s$
Cross section:	$A = 10^{-4}$	$cm^2$
Base width:	$W = 10^{-3}$	$cm$
Emitter length:	$L_E = 10^{-2}$	$cm$

Determine:

- The mobilities  $\mu_n$  and  $\mu_p$
- The diffusion coefficients  $D_n$  and  $D_p$
- The emitter efficiency factor  $\gamma$
- The transport factor  $\beta$
- The current gain  $\alpha$

### Solution

a. The mobilities are read from Fig. A-2 in Appendix A as

$$\begin{aligned}\mu_n &= 200 \text{ cm}^2/\text{V}\cdot\text{s} & \text{for } N_{dE} = 5 \times 10^{18} \text{ cm}^{-3} \\ \mu_p &= 500 \text{ cm}^2/\text{V}\cdot\text{s} & \text{for } N_a = 5 \times 10^{16} \text{ cm}^{-3}\end{aligned}$$

b. The diffusion coefficients are

$$\begin{aligned}D_n &= \mu_n V_T = 200 \times 26 \times 10^{-3} = 5.20 \text{ cm}^2/\text{s} \\ D_p &= 500 \times 26 \times 10^{-3} = 13.0 \text{ cm}^2/\text{s}\end{aligned}$$

c. The emitter efficiency factor is

$$\gamma = \left( 1 + \frac{13.0 \times 5 \times 10^{16} \times 10^{-3}}{5.20 \times 5 \times 10^{18} \times 10^{-2}} \right)^{-1} = 0.997$$

d. The transport factor is

$$\beta^* = 1 - \frac{(10^{-3})^2}{2 \times 10^{-6} \times 5.20} = 0.904$$

e. The current gain is

$$\alpha = \beta^* \gamma = 0.904 \times 0.997 = 0.90$$

**Common-emitter *n-p-n* transistor.** In the active region of a common-emitter *n-p-n* transistor, the emitter junction is forward-biased and the collector junction is reverse-biased. The base current is

$$I_B = -(I_C + I_E) \quad (5-1-53)$$

Combining this equation with Eq. (5-1-51), we have

$$I_C = \frac{-I_{CO}}{1 - \alpha} + \frac{\alpha I_B}{1 - \alpha} \quad (5-1-54)$$

In the cutoff region, if  $I_B = 0$ , then  $I_E = -I_C$  and the collector current is given by

$$I_C = -I_E = \frac{-I_{CO}}{1 - \alpha} = I_{CEO} \quad (5-1-55)$$

The actual collector current with the collector junction reverse-biased and the base junction open-circuited is designated by the symbol  $I_{CEO}$ . We define the common-emitter current gain  $\beta$  or  $h_{fe}$  as

$$\beta = h_{fe} = \frac{I_C + I_{CO}}{I_B} \quad (5-1-56)$$

Since  $I_E + I_B + I_C + I_{CO} = 0$ , we have

$$\beta = \frac{\alpha}{1 - \alpha} \quad (5-1-57)$$

### 5-1-5 Power-Frequency Limitations

The question then arises as to whether microwave power transistors have any limitations on their frequency and output power. The answer is yes. Several authors have discussed this subject. Early [4] first introduced the power-frequency limitations inherent in (1) the limiting velocity of carriers in semiconductors and (2) the maximum fields attainable in semiconductors without the onset of avalanche multiplication. These basic ideas were later developed and discussed in detail by Johnson [5], who made three assumptions:

1. There is a maximum possible velocity of carriers in a semiconductor. This is the "saturated drift velocity  $v_s$ " and is on the order of  $6 \times 10^6$  cm/s for electrons and holes in silicon and germanium.
2. There is a maximum electric field  $E_m$  that can be sustained in a semiconductor without having dielectric breakdown. This field is about  $10^5$  V/cm in germanium and  $2 \times 10^5$  V/cm in silicon.
3. The maximum current that a microwave power transistor can carry is limited by the base width.

With these three postulates Johnson derived four basic equations for the power-frequency limitations on microwave power transistors.

**First equation:** Voltage-Frequency Limitation:

$$V_m f_T = \frac{E_m v_s}{2\pi} = \begin{cases} 2 \times 10^{11} \text{ V/s for silicon} \\ 1 \times 10^{11} \text{ V/s for germanium} \end{cases} \quad (5-1-58)$$

where  $f_T = \frac{1}{2\pi\tau}$  is the charge-carrier transit-time cutoff frequency

$\tau = \frac{L}{v}$  is the average time for a charge carrier moving at an average velocity  $v$  to traverse the emitter-collector distance  $L$

$V_m = E_m L_{min}$  is the maximum allowable applied voltage

$v_s =$  maximum possible saturated drift velocity

$E_m =$  maximum electric field

With the carriers moving at a velocity  $v_s$  of  $6 \times 10^6$  cm/s, the transit time can

be reduced even further by decreasing the distance  $L$ . The lower limit on  $L$  can be reached when the electric field becomes equal to the dielectric breakdown field. However, the present state of the art of microwave transistor fabrication limits the emitter-collector length  $L$  to about  $25 \mu\text{m}$  for overlay and matrix devices and to nearly  $250 \mu\text{m}$  for interdigitated devices. Consequently, there is an upper limit on cutoff frequency. In practice, the attainable cutoff frequency is considerably less than the maximum possible frequency indicated by Eq. (5-1-58) because the saturated velocity  $v_s$  and the electric field intensity will not be uniform.

**Second equation:** Current-Frequency Limitation:

$$(I_m X_c) f_T = \frac{E_m v_s}{2\pi} \quad (5-1-59)$$

where  $I_m$  = maximum current of the device

$X_c = \frac{1}{\omega_T C_0} = \frac{1}{2\pi f_T C_0}$  is the reactive impedance

$C_0$  = collector-base capacitance

It should be noted that the relationship  $2\pi f_T \tau_0 \approx 2\pi f_T \tau = 1$  is used in deriving Eq. (5-1-59) from Eq. (5-1-58). In practice, no maximum current exists because the area of the device cannot be increased without bound. If the impedance level is zero, the maximum current through a velocity-saturated sample might be infinite. However, the limited impedance will limit the maximum current for a maximum attainable power.

**Third equation:** Power-Frequency Limitation:

$$(P_m X_c)^{1/2} f_T = \frac{E_m v_s}{2\pi} \quad (5-1-60)$$

This equation was obtained by multiplying Eq. (5-1-58) by Eq. (5-1-59) and replacing  $V_m I_m$  by  $P_m$ . It is significant that, for a given device impedance, the power capacity of a device must be decreased as the device cutoff frequency is increased. For a given product of  $E_m v_s$  (that is, a given material), the maximum power that can be delivered to the carriers traversing the transistor is infinite if the cross section of the transistor can be made as large as possible. In other words, the value of the reactance  $X_c$  must approach zero. Thus Eq. (5-1-60) allows the results to be predicted. Figure 5-1-13 shows a graph of Eq. (5-1-60) and the experimental results reported from manufacturers [6].

**Fourth equation:** Power Gain-Frequency Limitation:

$$(G_m V_{th} V_m)^{1/2} f = \frac{E_m v_s}{2\pi} \quad (5-1-61)$$

where  $G_m$  = maximum available power gain

$V_{th} = KT/e$  is the thermal voltage

$K$  = Boltzmann's constant,  $1.38 \times 10^{-23} \text{ J}^\circ\text{K}$

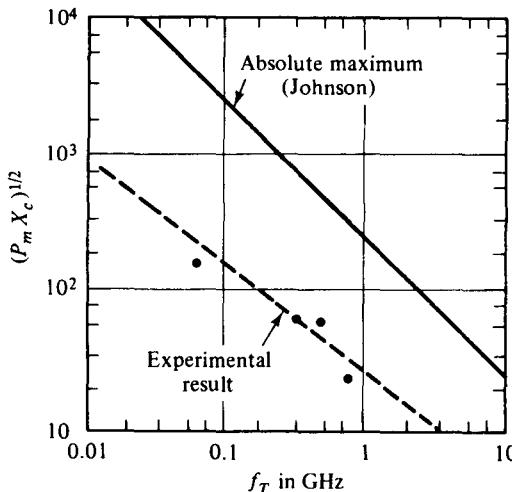


Figure 5-1-13  $(P_m X_c)^{1/2}$  versus  $f_T$ .  
(After B. C. De Loach [6]; reprinted by permission of Academic Press.)

$$T = \text{absolute temperature in degrees Kelvin}$$

$$e = \text{electron charge } (1.60 \times 10^{-19} \text{ C})$$

The maximum available power gain of a transistor was derived by Johnson [5] as

$$G_m = \left( \frac{f_T}{f} \right)^2 \frac{Z_{\text{out}}}{Z_{\text{in}}} \quad (5-1-62)$$

where  $Z_{\text{out}}$  and  $Z_{\text{in}}$  are the output and input impedances, respectively. If the electrode series resistances are assumed to be zero, the ratio of the output impedance to the input impedance can be written

$$\frac{Z_{\text{out}}}{Z_{\text{in}}} = \frac{C_{\text{in}}}{C_{\text{out}}} \quad (5-1-63)$$

where  $C_{\text{in}}$  is the input capacitance and  $C_{\text{out}}$  is the output (base-collector) capacitance. When the maximum total carrier charges  $Q_m$  move to the collector in a carrier-base transit time  $\tau_b$  and with a thermal voltage  $V_{\text{th}}$ , the input capacitance  $C_{\text{in}}$  and the emitter diffusion capacitance  $C_d$  are related by

$$C_{\text{in}} = C_d \approx \frac{Q_m}{V_{\text{th}}} = \frac{I_m \tau_b}{V_{\text{th}}} \quad (5-1-64)$$

The output capacitance is given by

$$C_{\text{out}} = \frac{I_m \tau_0}{V_m} \quad (5-1-65)$$

Substitution of Eqs. (5-1-58), (5-1-64), and (5-1-65) in Eq. (5-1-62) yields Eq. (5-1-61). The actual performance of a microwave transistor will fall far short of that predicted by Eq. (5-1-61). At present the high-frequency limit of a 28-V silicon  $n-p-n$  transistor operating at the 1-W level is approximately 10 GHz. Typical power gains of microwave transistors lie in the 6- to 10-dB range.

**Example 5-1-4: Power-Frequency Limitation**

A certain silicon microwave transistor has the following parameters:

Reactance:	$X_c = 1 \Omega$
Transit-time cutoff frequency:	$f_T = 4 \text{ GHz}$
Maximum electric field:	$E_m = 1.6 \times 10^5 \text{ V/cm}$
Saturation drift velocity:	$v_s = 4 \times 10^5 \text{ cm/s}$

Determine the maximum allowable power that the transistor can carry.

**Solution.** From Eq. (5-1-60) the maximum allowable power is

$$P_m = \frac{1}{X_c f_T^2} \left( \frac{E_m v_s}{2\pi} \right)^2 = \frac{1}{1 \times (4 \times 10^9)^2} \left( \frac{1.6 \times 10^5 \times 4 \times 10^5}{2\pi} \right)^2 = 6.48 \text{ W}$$

## 5-2 HETEROJUNCTION BIPOLAR TRANSISTORS (HBTs)

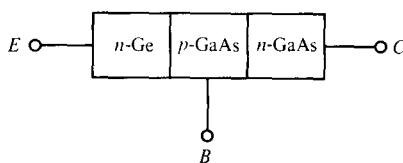
Bipolar transistors can be constructed as homojunction or heterojunction types of transistors. When the transistor junction is jointed by two similar materials such as silicon to silicon or germanium to germanium, it is a *homojunction transistor*. The transistor junction formed by two different materials, such as Ge to GaAs, is called a *heterojunction transistor*. So far only the ordinary homojunction transistors have been discussed. In this section we study the heterojunction transistors.

### 5-2-1 Physical Structures

When the lattice constants of two semiconductor materials are matched, they can be formed together as a heterojunction transistor. This lattice condition is very important because the lattice mismatch could introduce a large number of interface states and degrade the heterojunction operation. Currently, Ge and GaAs are the two materials commonly used for heterojunction structures because their lattice constants ( $a = 5.646 \text{ \AA}$  for Ge and  $a = 5.653 \text{ \AA}$  for GaAs) are matched to within 1%. Since each material may be either *p* type or *n* type, there are four possible heterojunction combinations:

1. *p*-Ge to *p*-GaAs junction
2. *p*-Ge to *n*-GaAs junction
3. *n*-Ge to *p*-GaAs junction
4. *n*-Ge to *n*-GaAs junction

Fig. 5-2-1 shows the model diagram of a heterojunction transistor formed by *n*-Ge, *p*-GaAs, and *n*-GaAs materials.



**Figure 5-2-1** Model diagram of a heterojunction transistor.

## **5-2-2 Operational Mechanism**

When an  $n$ -Ge and a  $p$ -GaAs are isolated, their Fermi energy levels are not aligned, as shown in Fig. 5-2-2 [7].

In Fig. 5-2-2, the vacuum level is used as reference, the work function is denoted by  $\phi$ ,  $n$ -Ge is designated as 1, and  $p$ -GaAs is referred to as 2. The different energies of the conduction-band edge and the valence-band edge are given by

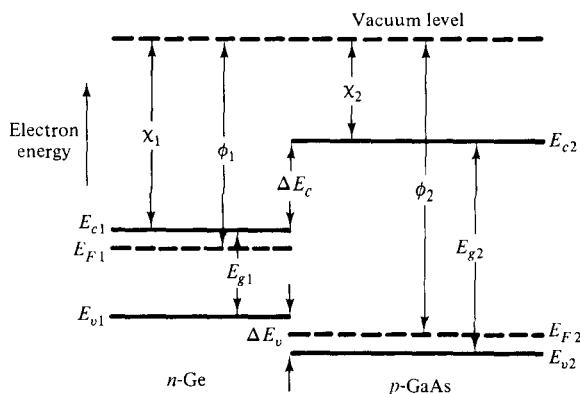
$$\Delta E_c = \chi_1 - \chi_2 \quad (5-2-1)$$

and

$$\Delta E_v = E_{g2} - E_{g1} - \Delta E_c \quad (5-2-2)$$

where  $\chi$  = electron affinity in eV

$E_g$  = bandgap energy in eV



**Figure 5-2-2** Energy-band diagram for isolated  $n$ -Ge and  $p$ -GaAs.

### Example 5-2-1: Heterojunction Bipolar Transistor (HBT)

A Ge-GaAs heterojunction transistor has the following parameters:

Lattice constant: Ge	$a_1 = 5.646$ Å
	$a_2 = 5.653$ Å
Electron affinity: Ge	$\chi_1 = 4.0$ eV
	$\chi_2 = 4.07$ eV
Energy gap: Ge	$E_{g1} = 0.80$ eV
	$E_{g2} = 1.43$ eV

Determine:

- The lattice match in percent
- The conduction-band differential between Ge and GaAs
- The valence-band differential between Ge and GaAs

**Solution**

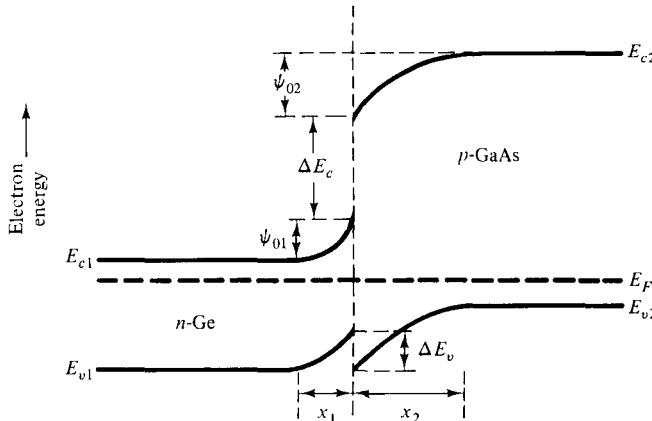
- The lattice match is within 1%
- The conduction-band differential is

$$\Delta E_c = \chi_1 - \chi_2 = 4.0 - 4.07 = -0.07 \text{ eV}$$

- The valence-band differential is

$$\begin{aligned} E_v &= E_{v2} - E_{v1} - \Delta E_c = 1.43 - 0.8 - (-0.07) \\ &= 0.70 \text{ eV} \end{aligned}$$

When the two semiconductor materials are jointed together, their Fermi energy levels are aligned and their energy bands are depleted at the junction, as shown in Fig. 5-2-3 [7].



**Figure 5-2-3** Energy-band diagram for an *n*-Ge-*p*-GaAs junction.

When the two materials are jointed together, the electrons in the *n*-Ge are injected into the *p*-GaAs, and the holes in the *p*-GaAs are transferred to the *n*-Ge until their Fermi energy levels are aligned. As a result, the energy bands at the junction are depleted or bent. The bending energy then creates a built-in voltage in both sides of the junction. The total built-in voltage is expressed by

$$\psi_o = \psi_{o1} + \psi_{o2} \quad (5-2-3)$$

where  $\psi_{o1}$  = barrier potential or portion of built-in voltage in *n*-Ge

$\psi_{o2}$  = barrier potential or portion of built-in voltage in *p*-GaAs

At the junction, the electric flux  $D$  is continuous. That is,

$$\begin{aligned} D &= \epsilon_0 \epsilon_{r1} \mathcal{E}_1 = \epsilon_0 \epsilon_{r2} \mathcal{E}_2 \\ &= \epsilon_1 \mathcal{E}_1 = \epsilon_2 \mathcal{E}_2 \end{aligned} \quad (5-2-4)$$

where  $\epsilon_0$  = permittivity of free space

$\epsilon$  = permittivity

$\epsilon_r$  = relative permittivity or dielectric constant

$\mathcal{E}$  = electric field

The space charges on both sides of the junction are equal and it is given by

$$x_1 N_d = x_2 N_a \quad (5-2-5)$$

where  $x_1$  = depletion width in  $n$ -Ge

$x_2$  = depletion width in  $p$ -GaAs

$N_d$  = donor density

$N_a$  = acceptor density

The electric fields in both sides can be written as

$$\mathcal{E}_1 = \frac{\psi_{o1} - V_1}{x_1} \quad (5-2-6)$$

and

$$\mathcal{E}_2 = \frac{\psi_{o2} - V_2}{x_2} \quad (5-2-7)$$

where  $V_1$  = portion of bias-voltage in  $n$ -Ge

$V_2$  = portion of bias-voltage in  $p$ -GaAs

Substitution of Eq. (5-2-4) into Eqs. (5-2-6) and (5-2-7) results in

$$(\psi_{o1} - V_1) \epsilon_{r1} N_{d1} = (\psi_{o2} - V_2) \epsilon_{r2} N_{a2} \quad (5-3-8)$$

For the heterojunction shown in Fig. 5-2-3, the electron current from  $n$ -Ge to  $p$ -GaAs is very small because the potential barrier of  $(\psi_{o1} + \psi_{o2} + \Delta E_c/q)$  across the junction for electron injection is very high. In contrast, the hole current from the  $p$ -GaAs side to the  $n$ -Ge side is dominant because of the low potential barrier  $\psi_{o2}$  for hole injection. Therefore, the junction current can be approximated as shown in Eq. (5-1-42) to be

$$I = \frac{A q D_p p_{no}}{L_p} (e^{V/V_T} - 1) \quad (5-2-9)$$

where  $A$  = cross section

$q$  = electron charge

$D_p$  = hole diffusion constant

$P_{no}$  = minority or equilibrium hole density in  $n$ -Ge

$L_p$  = hole diffusion length

$V$  = bias voltage

$V_T$  = voltage equivalent of temperature

### 5-2-3 Electronic Applications

Heterojunctions have been studied since 1951 and have many applications in photon devices as described in Chapter 10. The heterojunction bipolar transistor is a potential candidate for high-speed switching devices such as GaAs MESFETs. The analysis described previously can be applied to the structures of Ge-GaAs and GaAs-AlGaAs. In other heterojunction transistors, such as the Ge-Si structure, the lattice mismatch ( $a = 5.646 \text{ \AA}$  for Ge and  $a = 5.431 \text{ \AA}$  for Si) causes a high interface state density and recombination- and tunneling-current components must be counted.

---

#### Example 5-2-2: $n$ -Ge- $p$ -GaAs- $n$ -GaAs HBT

An  $n$ -Ge- $p$ -GaAs- $n$ -GaAs heterojunction transistor at  $300^\circ \text{ K}$  has the following parameters:

Donor density in $n$ -Ge region:	$N_d = 5 \times 10^{18} \text{ cm}^{-3}$
Acceptor density in $p$ -GaAs region:	$N_a = 6 \times 10^{16} \text{ cm}^{-3}$
Hole lifetime:	$\tau_p = 6 \times 10^{-6} \text{ sec}$
Bias voltage at emitter junction:	$V_E = 1 \text{ V}$
Cross section:	$A = 2 \times 10^{-2} \text{ cm}^2$

Compute:

- The built-in voltage in the  $p$ -GaAs side
- The hole mobility
- The hole diffusion constant
- The minority hole density in the  $n$ -Ge region
- The minority electron density in the  $p$ -GaAs region
- The hole diffusion length
- The emitter-junction current

#### Solution

- The built-in voltage in the  $p$ -GaAs side is

$$\psi_{02} = -26 \times 10^{-3} \ln \left( \frac{6 \times 10^{16}}{1.8 \times 10^6} \right) = -0.63 \text{ V}$$

- The hole mobility is read from Fig. A-2 in Appendix A as

$$\mu_p = 400 \text{ cm}^2/\text{V}\cdot\text{s}$$

- The hole diffusion constant is

$$D_p = 400 \times 26 \times 10^{-3} = 10.40 \text{ cm}^2/\text{s}$$

- The minority hole density in  $n$ -Ge is

$$P_{no} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{18}} = 45 \text{ cm}^{-3}$$

e. The minority electron density in the  $p$ -GaAs region is

$$n_{po} = \frac{(1.8 \times 10^6)^2}{6 \times 10^{16}} = 5.4 \times 10^{-3} \text{ cm}^{-3}$$

f. The hole diffusion length is

$$L_p = \sqrt{6 \times 10^{-6} \times 10.40} = 7.90 \times 10^{-3} \text{ cm}$$

g. The emitter-junction current is computed from Eq. (5-2-9) as

$$I = \frac{2 \times 10^{-2} \times 1.6 \times 10^{-19} \times 10.4 \times 45}{7.9 \times 10^{-3}} [e^{1/(26 \times 10^{-3})} - 1]$$

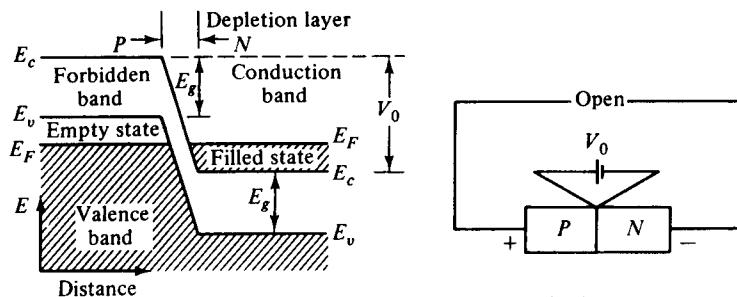
$$= 0.958 \text{ A}$$

### 5-3 MICROWAVE TUNNEL DIODES

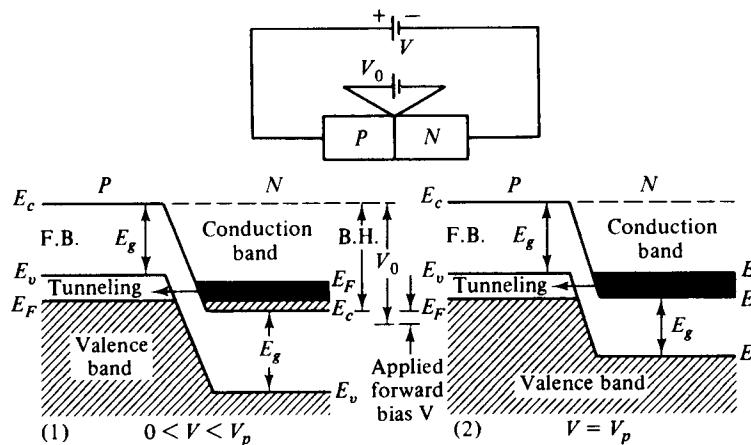
After the publication of Esaki's classic paper on tunnel diodes in 1958, the potential of tunnel diodes for microwave applications was quickly established. Prior to 1958 the anomalous characteristics of some  $p$ - $n$  junctions were observed by many scientists, but the irregularities were rejected immediately because they did not follow the "classic" diode equation. Esaki, however, described this anomalous phenomenon by applying a quantum tunneling theory. The tunneling phenomenon is a majority carrier effect. The tunneling time of carriers through the potential energy barrier is not governed by the classic transit-time concept—that the transit time is equal to the barrier width divided by the carrier velocity—but rather by the quantum transition probability per unit time. Tunnel diodes are useful in many circuit applications in microwave amplification, microwave oscillation, and binary memory because of their low cost, light weight, high speed, low-power operation, low noise, and high peak-current to valley-current ratio.

#### 5-3-1 Principles of Operation

The tunnel diode is a negative-resistance semiconductor  $p$ - $n$  junction diode. The negative resistance is created by the tunnel effect of electrons in the  $p$ - $n$  junction. The doping of both the  $p$  and  $n$  regions of the tunnel diode is very high—impurity concentrations of  $10^{19}$  to  $10^{20}$  atoms/cm $^3$  are used—and the depletion-layer barrier at the junction is very thin, on the order of 100 Å or  $10^{-6}$  cm. Classically, it is possible for those particles to pass over the barrier if and only if they have an energy equal to or greater than the height of the potential barrier. Quantum mechanically, however, if the barrier is less than 3 Å there is an appreciable probability that particles will tunnel through the potential barrier even though they do not have enough kinetic energy to pass over the same barrier. In addition to the barrier thinness, there must also be filled energy states on the side from which particles will tunnel and allowed empty states on the other side into which particles penetrate through at the same energy level. In order to understand the tunnel effects fully, let us analyze the energy-band pictures of a heavily doped  $p$ - $n$  diode. Figure 5-3-1 shows energy-band diagrams of a tunnel diode.



(a) Tunnel diode under zero-bias equilibrium



(b) Tunnel diode with applied forward bias

$E_F$  is the Fermi level representing the energy state with 50% probability of being filled if no forbidden band exists

$V_0$  is the potential barrier of the junction

$E_g$  is the energy required to break a covalent bond, which is 0.72 eV for germanium and 1.10 eV for silicon

$E_c$  is the lowest energy in the conduction band

$E_v$  is the maximum energy in the valence band

$V$  is the applied forward bias

F.B. stands for the forbidden band

B.H. represents the barrier height

Figure 5-3-1 Energy-band diagrams of tunnel diode.

Under open-circuit conditions or at zero-bias equilibrium, the upper levels of electron energy of both the *p* type and *n* type are lined up at the same Fermi level as shown in Fig. 5-3-1(a). Since there are no filled states on one side of the junction that are at the same energy level as empty allowed states on the other side, there is no flow of charge in either direction across the junction and the current is zero, as shown at point (a) of the volt-ampere characteristic curve of a tunnel diode in Fig. 5-3-2.

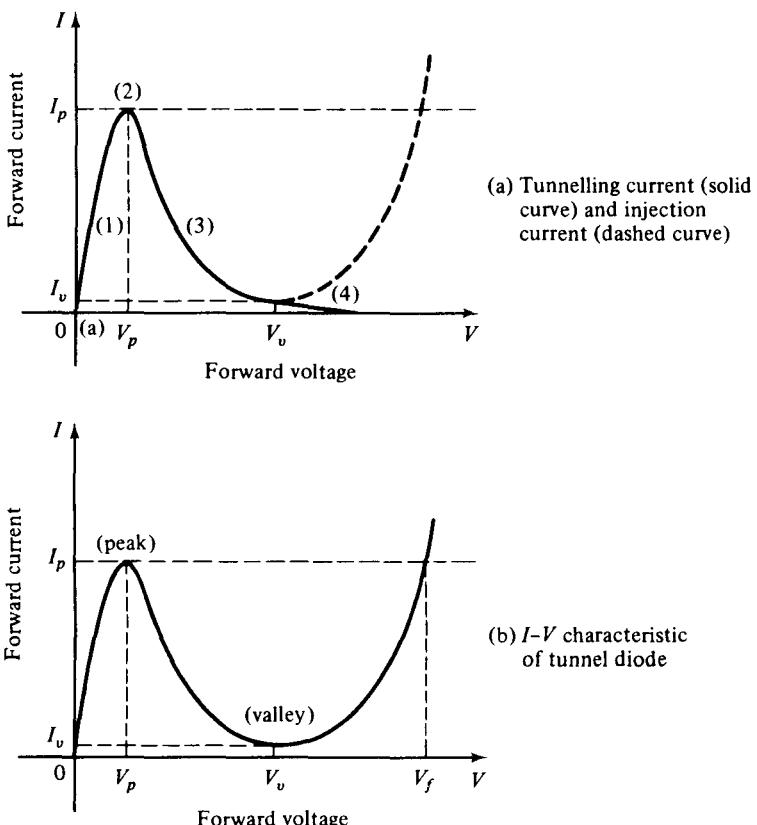


Figure 5-3-2 Ampere-voltage characteristics of tunnel diode.

In ordinary diodes the Fermi level exists in the forbidden band. Since the tunnel diode is heavily doped, the Fermi level exists in the valence band in *p*-type and in the conduction band in *n*-type semiconductors. When the tunnel diode is forward-biased by a voltage between zero and the value that would produce peak tunneling current  $I_p$  ( $0 < V < V_p$ ), the energy diagram is shown in part (1) of Fig. 5-3-1(b). Accordingly, the potential barrier is decreased by the magnitude of the applied forward-bias voltage. A difference in Fermi levels in both sides is created. Since there are filled states in the conduction band of the *n* type at the same energy level as allowed empty states in the valence band of the *p* type, the electrons tunnel through the barrier from the *n* type to the *p* type, giving rise to a forward tunneling current

from the *p* type to the *n* type as shown in sector (1) of Fig. 5-3-2(a). As the forward bias is increased to  $V_p$ , the picture of the energy band is as shown in part (2) of Fig. 5-3-1(b). A maximum number of electrons can tunnel through the barrier from the filled states in the *n* type to the empty states in the *p* type, giving rise to the peak current  $I_p$  in Fig. 5-3-2(a). If the bias voltage is further increased, the condition shown in part (3) of Fig. 5-3-1(b) is reached. The tunneling current decreases as shown in sector (3) of Fig. 5-3-2(a). Finally, at a very large bias voltage, the band structure of part (4) of Fig. 5-3-1(b) is obtained. Since there are now no allowed empty states in the *p* type at the same energy level as filled states in the *n* type, no electrons can tunnel through the barrier and the tunneling current drops to zero as shown at point (4) of Fig. 5-3-2(a).

When the forward-bias voltage  $V$  is increased above the valley voltage  $V_v$ , the ordinary injection current  $I$  at the *p-n* junction starts to flow. This injection current is increased exponentially with the forward voltage as indicated by the dashed curve of Fig. 5-3-2(a). The total current, given by the sum of the tunneling current and the injection current, results in the volt-ampere characteristic of the tunnel diode as shown in Fig. 5-3-2(b). It can be seen from the figure that the total current reaches a minimum value  $I_v$  (or valley current) somewhere in the region where the tunnel-diode characteristic meets the ordinary *p-n* diode characteristic. The ratio of peak current to valley current ( $I_p/I_v$ ) can theoretically reach 50 to 100. In practice, however, this ratio is about 15.

### 5-3-2 Microwave Characteristics

The tunnel diode is useful in microwave oscillators and amplifiers because the diode exhibits a negative-resistance characteristic in the region between peak current  $I_p$  and valley current  $I_v$ . The *I-V* characteristic of a tunnel diode with the load line is shown in Fig. 5-3-3.

Here the *abc* load line intersects the characteristic curve in three points. Points *a* and *c* are stable points, and point *b* is unstable. If the voltage and current vary about *b*, the final values of  $I$  and  $V$  would be given by point *a* or *c*, but not by *b*. Since the tunnel diode has two stable states for this load line, the circuit is called *bistable*, and it can be utilized as a binary device in switching circuits. However, mi-

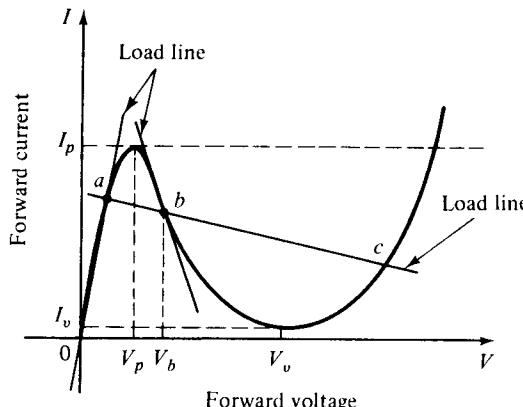


Figure 5-3-3 *I-V* characteristic of tunnel diode with load line.

crowave oscillation or amplification generated by the tunnel diode is our major concern in this section. The second load line intersects the  $I$ - $V$  curve at point  $b$  only. This point is stable and shows a dynamic negative conductance that enables the tunnel diode to function as a microwave amplifier or oscillator. The circuit with a load line crossing point  $b$  in the negative-resistance region is called *astable*. Another load line crossing point  $a$  in the positive-resistance region indicates a *monostable* circuit. The negative conductance in Fig. 5-3-3 is given by

$$-g = \frac{\partial i}{\partial v} \bigg|_{v_b} = \frac{1}{-R_n} \quad (5-3-1)$$

where  $R_n$  is the magnitude of negative resistance.

For a small variation of the forward voltage about  $V_b$ , the negative resistance is constant and the diode circuit behavior is stable. A small-signal equivalent circuit for the tunnel diode operated in the negative-resistance region is shown in Fig. 5-3-4. Here  $R_s$  and  $L_s$  denote the inductance and resistance of the packaging circuit of a tunnel diode. The junction capacitance  $C$  of the diode is usually measured at the valley point;  $R_n$  is the negative resistance of the diode. Typical values of these parameters for a tunnel diode having a peak current  $I_p$  of 10 mA are

$$-R_n = -30 \Omega \quad R_s = 1 \Omega \quad L_s = 5 \text{ nH} \quad C = 20 \text{ pF}$$

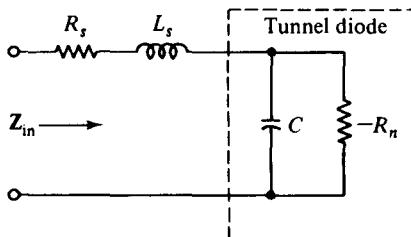


Figure 5-3-4 Equivalent circuit of tunnel diode.

The input impedance  $Z_{in}$  of the equivalent circuit shown in Fig. 5-3-4 is given by

$$Z_{in} = R_s + j\omega L_s + \frac{R_n[j/(\omega C)]}{-R_n - j/(\omega C)} \quad (5-3-2)$$

$$Z_{in} = R_s - \frac{R_n}{1 + (\omega R_n C)^2} + j \left[ \omega L_s - \frac{\omega R_n^2 C}{1 + (\omega R_n C)^2} \right] \quad (5-3-2)$$

For the resistive cutoff frequency, the real part of the input impedance  $Z_{in}$  must be zero. Consequently, from Eq. (5-3-2) the resistive cutoff frequency is given by

$$f_c = \frac{1}{2\pi R_n C} \sqrt{\frac{R_n}{R_s}} - 1 \quad (5-3-3)$$

For the self-resonance frequency, the imaginary part of the input impedance must be zero. Thus,

$$f_r = \frac{1}{2\pi R_n C} \sqrt{\frac{R_n^2 C}{L_s}} - 1 \quad (5-3-4)$$

The tunnel diode can be connected either in parallel or in series with a resistive load as an amplifier; its equivalent circuits are shown in Fig. 5-3-5.

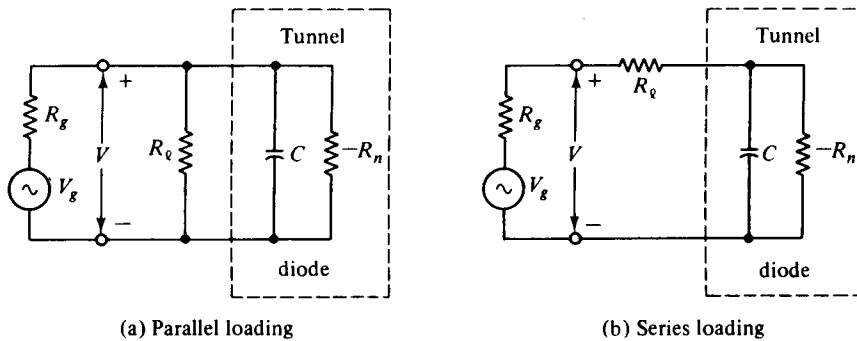


Figure 5-3-5 Equivalent circuits of tunnel diodes.

**Parallel loading.** It can be seen from Fig. 5-3-5(a) that the output power in the load resistance is given by

$$P_{\text{out}} = \frac{V^2}{R_\ell} \quad (5-3-5)$$

One part of this output power is generated by the small input power through the tunnel diode amplifier with a gain of  $A$ , and this part can be written

$$P_{\text{in}} = \frac{V^2}{AR_\ell} \quad (5-3-6)$$

Another part of the output power is generated by the negative resistance, and it is expressed as

$$P_n = \frac{V^2}{R_n} \quad (5-3-7)$$

Therefore

$$\frac{V^2}{AR_\ell} + \frac{V^2}{R_n} = \frac{V^2}{R_\ell} \quad (5-3-8)$$

and the gain equation of a tunnel diode amplifier is given by

$$A = \frac{R_n}{R_n - R_\ell} \quad (5-3-9)$$

When the negative resistance  $R_n$  of the tunnel diode approaches the load resistance  $R_\ell$ , the gain  $A$  approaches infinity and the system goes into oscillation.

**Series loading.** In the series circuit shown in Fig. 5-3-5(b) the power gain  $A$  is given by

$$A = \frac{R_\ell}{R_\ell - R_n} = \frac{1}{1 - R_n/R_\ell} \quad (5-3-10)$$

The device remains stable in the negative-resistance region without switching if  $R_\ell < R_n$ .

A tunnel diode can be connected to a microwave circulator to make a negative-resistance amplifier as shown in Fig. 5-3-6. A microwave circulator is a multiport junction in which the power may flow only from port 1 to port 2, port 2 to port 3, and so on in the direction shown. Although the number of ports is not restricted, microwave circulators with four ports are most commonly used. If the circulator is perfect and has a positive real characteristic impedance  $R_0$ , an amplifier with infinite gain can be built by selecting a negative-resistance tunnel diode whose input impedance has a real part equal to  $-R_0$  and an imaginary part equal to zero. The reflection coefficient from Fig. 5-3-6 is infinite. In general, the reflection coefficient is given by

$$\Gamma = \frac{-R_n - R_0}{-R_n + R_0} \quad (5-3-11)$$

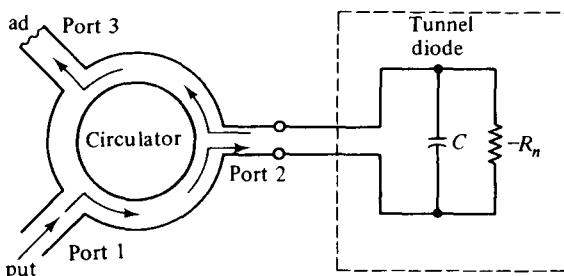


Figure 5-3-6 Tunnel diode connected to circulator.

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## PROBLEMS

### Microwave Bipolar Transistors

5-1. A GaAs n-p-n transistor at 300° K has the following parameters:

Base width	$W = 2 \times 10^{-5}$ cm
Diffusion length in emitter	$L_E = 2 \times 10^{-4}$ cm
Diffusion length in collector	$L_C = 4 \times 10^{-4}$ cm
Base resistivity	$\rho_B = 20 \Omega\text{-cm}$
Emitter resistivity	$\rho_E = 1 \Omega\text{-cm}$
Collector resistivity	$\rho_C = 10 \Omega\text{-cm}$
Emitter junction voltage	$V_E = 0.4$ V
Collector junction voltage	$V_C = 0.5$ V
Cross-section area	$A = 0.01 \text{ cm}^2$

Find: a. the impurity densities in the emitter, base and collector  
 b. the mobilities in the emitter, base, and collector  
 c. the diffusion lengths in the emitter, base, and collector  
 d. the equilibrium densities in the emitter, base, and collector  
 e. the coupling coefficients  
 f. the emitter and collector currents

5-2. Derive Eq. (5-1-30) from Eq. (5-1-27).

5-3. Derive Eq. (5-1-31) from Eq. (5-1-30).

5-4. Verify Eq. (5-1-34).

5-5. Derive Eqs. (5-1-39), (5-1-40), and (5-1-41).

5-6. A certain silicon bipolar transistor has a maximum electric field intensity  $E_m$  of  $3 \times 10^5$  volts/cm and its carrier has a saturated drift velocity  $v_s$  of  $4 \times 10^6$  cm/sec. The emitter-collector length  $L$  is 4 microns.

- Calculate the maximum allowable applied voltage.
- Compute the transit time for a charge to transverse the emitter-collector length  $L$ .
- Determine the maximum possible transit frequency.

**5-7.** A bipolar transistor has voltage-frequency and current-frequency limitations as shown in Eqs. (5-1-58) and (5-1-59). Derive the power-frequency limitation as shown in Eq. (5-1-60).

**5-8.** A bipolar transistor has a voltage-current-power limitation. Derive the power gain-frequency relationship as shown in Eq. (5-1-61).

### Heterojunction Bipolar Transistors

**5-9.** An *n*-Ge-*p*-GaAs-*n*-GaAs heterojunction transistor at 300° K has the following parameters:

Donor density in the <i>n</i> -Ge region:	$N_d = 2 \times 10^{19} \text{ cm}^{-3}$
Acceptor density in <i>p</i> -GaAs region:	$N_a = 3 \times 10^{17} \text{ cm}^{-3}$
Hole lifetime:	$\tau_p = 4 \times 10^{-6} \text{ sec}$
Bias voltage at emitter junction:	$V_E = 1.50 \text{ V}$
Cross section:	$A = 4 \times 10^{-2} \text{ cm}^2$

Compute: **a.** The built-in voltage in the *p*-GaAs side  
**b.** The hole mobility (read the value from Fig. 2-4-2)  
**c.** The hole diffusion constant  
**d.** The minority hole density in the *n*-Ge region  
**e.** The minority electron density in the *p*-GaAs region  
**f.** The hole diffusion length  
**g.** The emitter-junction current

**5-10.** An *n*-Ge-*p*-GaAs-*n*-GaAs heterojunction transistor at 300° K has the following parameters:

Donor density in the <i>n</i> -Ge region:	$N_d = 5 \times 10^{18} \text{ cm}^{-3}$
Acceptor density in the <i>p</i> -GaAs region:	$N_a = 6 \times 10^{16} \text{ cm}^{-3}$
Hole lifetime:	$\tau_p = 4 \times 10^{-6} \text{ sec}$
Bias voltage across <i>n-p</i> junction:	$V_E = 0.80 \text{ V}$
Cross section:	$A = 2 \times 10^{-2} \text{ cm}^2$

Calculate: **a.** The built-in voltage in the *p*-GaAs side  
**b.** The hole mobility (read from Fig. A-2 in Appendix A)  
**c.** The hole diffusion constant  
**d.** The minority hole density in the *n*-Ge region  
**e.** The minority electron density in the *p*-GaAs region  
**f.** The hole diffusion length  
**g.** The emitter-junction current

Describe the electronic applications of an HBT.

### Tunnel Diodes

**5-11.** A negative-resistance device is connected through a 1-kΩ resistor in series and a 0.01-μF capacitor in parallel to a combination of a supply voltage *V* of 10 V and a sig-

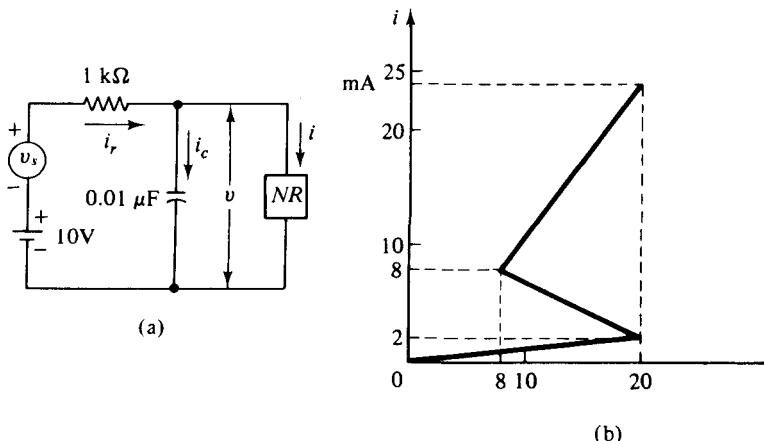


Figure P5-11

nal source  $V_s$  as shown in Fig. P5-11(a). Its I-V characteristic curve is shown in Fig. P5-11(b).

- Find the negative resistance and forward resistances of the device.
- Draw the load line on the I-V curve.
- Determine the quiescent operating point of the circuit by the values of voltage and current.
- Determine the new operating point by the values of voltage and current when a signal voltage of 14 V is applied to the circuit.
- Draw the new load line on the I-V curve.
- Find the time constant of the circuit.
- Compute  $v$ ,  $i$ ,  $i_c$ , and  $i_r$  as a function of time after the triggering signal is applied and before the transition takes place.
- Find the transition time  $T$  in microseconds.
- Calculate  $v$ ,  $i$ ,  $i_c$ , and  $i_r$  immediately after transition.

**5-12.** A microwave tunnel diode has a negative resistance  $R_n$  and the resonant circuit has a circuit resistance  $R_L$ . Derive an equation for the gain of a microwave tunnel-diode amplifier.

**5-13.** A certain microwave tunnel diode has a negative resistance of  $69 + j9.7 \Omega$ . Determine the resonant-circuit impedance so that the microwave tunnel-diode amplifier will produce a power gain of 15 dB.